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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/587,496	06/02/2000	Brian Bailey		7286

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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 08/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/587,496	BAILEY ET AL.	
	Examiner	Art Unit	
	Ayal I Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-25 of U.S. Application 09/587,496 filed on 06/02/2000 are presented for examination. Applicant's amendment, filed 04/22/2004, amended claims 1 and 20-23. Claims 24 and 25 have been added.

Drawings

2. The draftsperson has objected to the drawings submitted on 06/02/0000. Please see form PTO-948 for details of the objections.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S.

patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. The prior art used for these rejections is as follows:

5. Wang et al. U.S. Patent 6,134,516. (Henceforth referred to as "**Wang**").

6. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

7. **Claims 1-8 and 10-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang (U.S. Patent 6,134,516).**

8. In regards to claim 1, Wang teaches the following limitations:

> 1. A method comprising:
> retrieving state configuration information from a state server of a hardware/software co-simulation, wherein the hardware/software co-simulation simulates a software component of a system being executed and interacting with a hardware component of the system; and
> providing a client of the hardware/software co-simulation access to a server state of the state server based on the state configuration information.
> (Wang, especially: Abstract; col.3, line 55 –col.4, line 7; col.6, lines 56-67; col.7, lines 25-49; col.10, lines 15-17 and Fig.55; col.14, line 33 – col.15, line 2; col.78, line 63 – col.79, line 11; col.81, lines 1-17; col.81, line 26-47; col.83, line 37 – col.84, line 55;)

9. In regards to claim 2, Wang teaches the following limitations:

> 2. The method of claim 1 wherein the state server defines an address space or a virtual address space in the hardware/software co-simulation.
> (Wang, especially: Fig.3, Items 210, 215, 220; Figs.11-15 and col.8, lines 34-46;)

Wang expressly teaches a compiler in Fig.3. The feature of defining an address space is inherent to a compiler's work. Figs.11-15 of Wang show the use of "address points", which would not be able to function if there were no address space defined.

10. In regards to claim 3, Wang teaches the following limitations:

3. The method of claim 1 wherein the state configuration information comprises at least one of symbol allocation and symbol type.
(Wang, especially: Fig.3, Items 210, 215, 220)

Wang expressly teaches a compiler in Fig.3. The feature of allocating symbols to an address space is inherent to a compiler's work. Figs.11-15 of Wang show symbols allocated to "address points".

11. In regards to claim 4,

4. The method of claim 1 further comprising: registering the client with a co-simulation interface; and associating the client with at least one state server in the hardware/software co-simulation.
(Wang, especially: Fig.55, and col.10, lines 15-17; Figs.47-48 and col.83, line 37 to col.84, line 41;)

12. In regards to claim 5,

5. The method of claim 4 wherein registering the client comprises assigning the client a client identifier.
(Wang, especially: col.83, line 37 to col.84, line 65;)

Col.84, line 62 expressly referrs to a "owner identification".

13. In regards to claim 6,

6. The method of claim 4 wherein associating the client with at least one state server comprises providing the client with a list of available state servers and one or more address spaces associated with each of the available state server.
(Wang, especially: col.83, line 37 to col.84, line 65;)

14. In regards to claim 7,

7. The method of claim 6 wherein said client is to retain an identifier for at least one address space from the list.
(Wang, especially: col.83, line 37 to col.84, line 65;)

15. In regards to claim 8,

8. The method of claim 6 wherein said client is to return a selection from the list and wherein associating the client with at least one state server further comprises providing the client an identifier for at least one address space from the list based on the selection.
(Wang, especially: col.83, line 37 to col.84, line 65;)

16. In regards to claim 10,

10. The method of claim 1 further comprising: requesting the state configuration information, said state configuration information to define at least one memory location comprising the server state.
(Wang, especially: col.83, line 37 to col.84, line 65;)

17. In regards to claim 11,

11. The method of claim 10 wherein requesting the state configuration information comprises: receiving a client identifier for the client at a co-simulation interface;

receiving an identifier for an address space at the co-simulation interface, said server state being within the address space;
(Wang, especially: col.83, line 37 to col.84, line 65;)

and issuing a request from the co-simulation interface, said request including the client identifier and the identifier for the address space.
(Wang, especially: col.83, line 37 to col.84, line 65;)

18. In regards to claim 12,

12. The method of claim 11 wherein the request is to be serviced by the state server, said state sever to access a symbol table indicated by the identifier for the address space and to provide the state configuration information based on the symbol table.
(Wang, especially: col.83, line 37 to col.88, line 48;)

19. In regards to claim 13,

13. The method of claim 11 where a path of the request comprises a hardware kernel, a bus interface module within a logic simulator, an interprocess connection, a co-simulation manager within a software kernel, an instruction set simulator, and a debugger.
(Wang, especially: col.23, lines 15-25; col.83, line 37 to col.84, line 65; col.86, lines 21-50)

20. In regards to claim 14,

14. The method of claim 1 wherein providing the client access comprises: performing a memory operation on at least one memory location based on the state configuration information.
(Wang, especially: col.83, line 37 to col.88, line 48;)

21. In regards to claim 15,

15. The method of claim 14 wherein performing the memory operation comprises at least one of: reading the server state; modifying the server state; receiving the server state at a predetermined future time; and receiving notification upon a predetermined action on the server state.
(Wang, especially: col.83, line 37 to col.88, line 48;)

22. In regards to claim 16,

16. The method of claim 14 wherein performing the memory operation comprises:
generating a request for the memory operation, said request including a memory allocation from the state configuration information; accessing a memory map; and
(Wang, especially: col.83, line 37 to col.88, line 48;)

issuing the memory operation to a unified memory for the hardware/software cosimulation based on the memory allocation and the memory map.
(Wang, especially: col.83, line 37 to col.88, line 48;)

23. In regards to claim 17,

17. The method of claim 16 further comprising: receiving data in response to the memory operation; and interpreting the data based on a symbol type defined by the state configuration information.
(Wang, especially: col.83, line 37 to col.88, line 48;)

24. In regards to claim 18,

18. The method of claim 1 further comprising:

receiving stimulus based on the server state;
(Wang, especially: col.3, line 55 –col.4, line 7; Abstract; col.6, lines 56-67; col.7, lines 25-49; col.10, lines 15-17 and Fig.55; col.14, line 33 – col.15, line 2; col.78, line 63 – col.79, line 11; col.81, lines 1-17; col.81, line 26-47; col.83, line 37 – col.84, line 55;)

and applying the stimulus to the hardware/software co-simulation.
(Wang, especially: col.3, line 55 –col.4, line 7; Abstract; col.6, lines 56-67; col.7, lines 25-49; col.10, lines 15-17 and Fig.55; col.14, line 33 – col.15, line 2; col.78, line 63 – col.79, line 11; col.81, lines 1-17; col.81, line 26-47; col.83, line 37 – col.84, line 55;)

25. In regards to claim 19,

19. The method of claim 18 wherein the stimulus comprises data to be injected into the hardware/software co-simulation in response to a predetermined condition associated with the server state.
(Wang, especially: col.3, line 55 –col.4, line 7; Abstract; col.6, lines 56-67; col.7, lines 25-49; col.10, lines 15-17 and Fig.55; col.14, line 33 – col.15, line 2; col.78, line 63 – col.79, line 11; col.81, lines 1-17; col.81, line 26-47; col.83, line 37 – col.84, line 55;)

26. In regards to claim 20, Wang teaches the following limitations:

20. A method comprising:
accessing a software state from a hardware simulation process in a hardware/software co-simulation, wherein the hardware/software co-simulation simulates a software component of a system being executed and interacting with a hardware component of the system;.
(Wang, especially: col.3, line 55 –col.4, line 7; Abstract; col.6, lines 56-67; col.7, lines 25-49; col.10, lines 15-17 and Fig.55; col.14, line 33 – col.15, line 2; col.78, line 63 – col.79, line 11; col.81, lines 1-17; col.81, line 26-47; col.83, line 37 – col.84, line 55;)

27. In regards to claim 21, Wang teaches the following limitations:

21. A machine readable storage medium having stored thereon machine executable instructions, execution of said machine executable instructions to implement a method comprising:

retrieving state configuration information from a state server of a hardware/software co-simulator, wherein the hardware/software co-simulation simulates a software component of a system being executed and interacting with a hardware component of the system;; and
(Wang, especially: Abstract; col.3, line 55 –col.4, line 7; col.6, lines 56-67; col.7, lines 25-49; col.10, lines 15-17 and Fig.55; col.14, line 33 – col.15, line 2; col.78, line 63 – col.79, line 11; col.81, lines 1-17; col.81, line 26-47; col.83, line 37 – col.84, line 55;)

providing a client of the hardware/software co-simulator access to a server state of the state server based on the state configuration information.
(Wang, especially: Abstract; col.3, line 55 –col.4, line 7; col.6, lines 56-67; col.7, lines 25-49; col.10, lines 15-17 and Fig.55; col.14, line 33 – col.15, line 2; col.78, line 63 – col.79, line 11; col.81, lines 1-17; col.81, line 26-47; col.83, line 37 – col.84, line 55;)

28. In regards to claim 22, Wang teaches the following limitations:

22. A machine readable storage medium having stored thereon machine executable instructions, execution of said machine executable instructions to implement a method comprising:
accessing a software state from a hardware simulation process in a hardware/software co-simulation wherein the hardware/software co-simulation simulates a software component of a system being executed and interacting with a hardware component of the system.
(Wang, especially: Abstract; col.3, line 55 –col.4, line 7; col.6, lines 56-67; col.7, lines 25-49; col.10, lines 15-17 and Fig.55; col.14, line 33 – col.15, line 2; col.78, line 63 – col.79, line 11; col.81, lines 1-17; col.81, line 26-47; col.83, line 37 – col.84, line 55;)

29. In regards to claim 23, Wang teaches the following limitations:

23. An apparatus comprising:
a hardware/software co-simulator to retrieve state configuration information from a state server, wherein the hardware/software co-simulation simulates a software component of a system being executed and interacting with a hardware component of the system; and
a unified memory store, said hardware/software co-simulator to provide a client access to a server state of the state server within the unified memory store based on the state configuration information.
(Wang, especially: Abstract; col.3, line 55 –col.4, line 7; col.6, lines 56-67; col.7, lines 25-49; col.10, lines 15-17 and Fig.55; col.14, line 33 – col.15, line 2; col.78, line 63 – col.79, line 11; col.81, lines 1-17; col.81, line 26-47; col.83, line 37 – col.84, line 55;)

30. In regards to claim 24, Wang teaches the following limitations:

24. The method of claim 1, wherein the hardware/software co-simulation simulates the software component being executed by a microprocessor.
(Wang, especially: Abstract; col.3, line 55 –col.4, line 7; col.6, lines 56-67; col.7, lines 25-49; col.10, lines 15-17 and Fig.55; col.14, line 33 – col.15, line 2; col.78, line 63 – col.79, line 11; col.81, lines 1-17; col.81, line 26-47; col.83, line 37 – col.84, line 55;)

Claim Rejections - 35 USC § 103

31. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

32. The prior art used for these rejections is as follows:

33. Wang et al. U.S. Patent 6,134,516. (Henceforth referred to as "**Wang**").

34. Klein et al., U.S. Patent 5,768,567. (Henceforth referred to as "**Klein**").

35. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

36. Claims 9 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (U.S. Patent 6,134,516) in view of Klein (U.S. Patent 5,768,567).

37. In regards to claim 9, Wang does not expressly teach the following limitations:

9. The method of claim 1 wherein the state server comprises an instruction set simulator (ISS) and a bus interface model (BIM).

However, Klein does expressly teach these limitations. (See col.1 – col.2, "Background of the Invention").

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the teachings of Wang with the teachings of

Klein by incorporating a bus interface model (BIM), because "For the more 'complex' hardware, since it is very difficult, if not outright impossible, to model all the behaviors of the hardware, certain accuracy are often sacrificed. For example, in the case of a microprocessor, it is often modeled by a 'bus interface model', i.e. only the different bus cycles that the processor can execute are modeled." (Klein, col.1, lines 55-61)

Moreover, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the teachings of Wang with the teachings of Klein by incorporating an instruction set simulator (ISS), because "Embedded systems that are most difficult to validate are those that are neither software or hardware dominant, in that both parts play an equally important role in the success of the system. Due to increased market pressures, hardware and software are usually developed in parallel. Typically, the hardware designers would validate the hardware design using an hardware simulator or emulator. Concurrently, the software designer would validate the software using an instruction set simulator [ISS] on a general purpose computer." (Klein, col.1, line 65 – col.2, line 7).

38. In regards to claim 25, Wang does not expressly teach the following limitations:

25. The method of claim 9, wherein the ISS and the BIM simulate a microprocessor, the ISS executing instructions and the BIM representing input and output behavior as pin signals on a bus.

However, Klein does expressly teach these limitations. (See col.1 – col.2, "Background of the Invention"). In regards to BIM, Klein expressly teaches (col.1, lines 59-65) that:

> For example, in the case of a microprocessor, it is often modeled by a "bus interface model", i.e. only the different bus cycles that the processor can execute are modeled. The modeled bus cycles are driven in timed sequences, representative of typical bus transactions or bus activities for invoking specific conditions.

Examiner interprets "bus transactions" and "bus activities" as corresponding to changes in the individual pin signals that constitute a bus. In addition, in regards to ISS, Klein teaches that (col.2, lines 5-17):

> Concurrently, the software designer would validate the software using an instruction set simulator on a general purpose computer. The instruction set simulator simulates execution of compiled assembly/machine code for determining software correctness and performance at a gross level. These instruction set simulators often include facilitates for handling I/O data streams to simulate to a very limited degree the external hardware of the target design. Typically, instruction set simulators run at a speeds of ten thousand to several hundred thousand instructions per second, based on their level of detail and the performance of the host computer that they are being run on.

Examiner finds that "The instruction set simulator simulates execution of compiled assembly/machine code" corresponds to the claimed "... the ISS executing instructions ..."

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the teachings of Wang with the teachings of Klein by incorporating an instruction set simulator (ISS), because "Embedded systems that are most difficult to validate are those that are neither software or hardware dominant, in that both parts play an equally important role in the success of the system. Due to increased market pressures, hardware and software are usually developed in parallel. Typically, the hardware designers would validate the hardware design using an hardware simulator or emulator. Concurrently, the software designer would validate the software using an

instruction set simulator [ISS] on a general purpose computer." (Klein, col.1, line 65 – col.2, line 7).

Response to Amendment filed 4/22/2004

39. Applicants unpersuasively argue in the amendment (p.9) that:

> Wang does not teach or suggest a hardware/software co-simulation or co-simulator wherein the hardware/software co-simulation or co-simulator "simulates a software component of a system being executed and interacting with a hardware component of the system" as recited in independent claims 1 and 21.
>
> Wang is understood to disclose a system for simulating electronic designs by providing users of the system the ability to turn their designs into software and hardware representations for simulation. (Wang, col. 3, lines 55-58). Thus, as used in Wang, the term "co-simulation" refers to using a combination of a hardware emulator/accelerator and a software simulator to simulate and debug a particular circuit design. (Wang, col.. 3, lines 38-43).
>
> Further, as defined in Wang, the "circuit design" or "electronic design" that is simulated by the disclosed system is a custom designed system or component, whether software hardware, which can be modeled by the SEmulation system for test/debug purposes." (Wang, col.11, lines 1-5) (emphasis added).
>
> Thus, Wang is understood to be limited to simulating hardware or software, but not software being executed in a system and interacting with hardware of the system.

40. Examiner respectfully disagrees with Applicants' assertion. Wang teaches four (4) basic modes of operation: (1) software simulation, (2) simulation via hardware acceleration, (3) in-circuit emulation (ICE), and (4) post-simulation analysis, as well various combinations of these four basic modes. (See col. 4, lines 8-32).

41. Therefore, the following Applicants' assertion is incorrect: "... Thus, as used in Wang, the term 'co-simulation' refers to using a combination of a hardware emulator/accelerator and a software simulator to simulate and debug a particular circuit design." The mode of in-circuit emulation can be performed independently of software simulation. This point is expressly taught in col.4, line 8 – col.5, line 7, and shown in Fig.2, Item 150, and also Fig.1, Items 20, 61, and 70.

42. Applicants also argue in the amendment (p.9) that:

> By contrast, the present application is concerned with a different type of "co-simulation" known in the field of electronic design automation. Specifically, the claims of the present application are directed to hardware/software co-simulation wherein the hardware/software co-simulation simulates "a software component of a system being executed and interacting with a hardware component of the system." For example, as described in the Specification, embodiments of the disclosed hardware/software co-simulator can be used to simulate "a microprocessor, some memory devices, and special-purpose hardware 117 [, wherein the] simulated microprocessor executes software 161 stored in the simulated memory devices."
> (Specification, pg. 9, 1ines.1-7).

43. Examiner finds that In-Circuit Emulation (ICE) as taught by Wang, and as is well known in the art, constitutes one embodiment of the newly claimed limitation, "a software component of a system being executed and interacting with a hardware component of the system." Wang's description of the ICE mode is as follows (See col.6, lines 25-25):

> For the in-circuit emulation mode, the method comprises: (1) generating a software model of the circuit; (2) generating a hardware model of at least a portion of the circuit; (3) providing input signals from the target system to the hardware model; (4) providing output signals from the hardware model to the target system; (5) simulating a behavior of the circuit with the hardware model, where the software model is capable of controlling the simulation/emulation, cycle by cycle.

Examiner finds that the above cited section, especially item (5), teaches the claimed limitation of "a software component of a system being executed and interacting with a hardware component of the system."

44. In regards to Claims 2 and 3, Applicants state in the specification (p.7, lines 10-13) that "Software is written in a programming language that needs to be compiled by a compiler before it can be executed on a processor. Part of the job of the compiler is to allocate symbols to addresses." Wang expressly teaches a compiler in Fig.3. The features of defining an address space, and of symbol allocation are, according to Applicants' admission, inherent.

45. Examiner is therefore maintaining all rejections based on Wang.

Request for Examiner Interview

46. In the amendment filed on 4/22/04, Applicants request an Examiner Interview under MPEP §713.01. Examiner contacted the Applicant's representative on 7/14/04 and noted that MPEP §713.01 requires that the Applicants submit an agenda for the interview. Examiner stated that he would grant an after-final interview upon Applicants' submission of an agenda for an interview, which would be after Applicants' review of this Office Action. Applicant's Representative agreed to this.

Conclusion

47. Applicant's arguments filed 04/22/2004 have been fully considered but they are not persuasive.

48. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (703) 306-0297. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

4th floor receptionist's office
Crystal Park 2
2121 Crystal Drive
Arlington, VA

Fax: (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is: (703) 305-3900.

Ayal I. Sharon

Art Unit 2123

July 16, 2004